Reliability Analysis for VLSI Electronic Systems

Christopher M. Snowden, Roger D. Pollard

Microwave Solid State Group, Department of Electrical and Electronic Engineering,
University of Leeds, Leeds LS2 9JT, Great Britain

and

Patrick D. T. O'Connor

British Aerospace Dynamics Group,
PO Box 19, Six Hills Way, Stevenage SG1 8JU, Great Britain

(Received: 3 October 1985)

ABSTRACT

The standard methods used for analysing the reliability of electronic systems are unsuited to VLSI systems because of their large-scale and software-driven nature. In this paper, a review of the problems is presented together with an analysis of the difficulties encountered in extrapolation of the present techniques. Some proposals are presented with the intention of making the solution more manageable for this type of problem. Early results are given to suggest how the approach may develop.

1 INTRODUCTION

At present the only comprehensive and widely accepted technique for reliability prediction of electronic systems is based on the US Military Handbook 217D (MIL-HDBK-217D), produced by the US Department of Defense, which has been in worldwide use for many years. The technique uses standard formulae for the failure rates of individual
components and adds weighting factors for the various stresses which contribute to the occurrence of faults. The models are based on the assumption that if the failure rate contribution of each component can be assessed, then the overall failure rate of the system can be obtained as the weighted sum of the individual failure rates. Such arrangements were developed when electronic parts were simpler than present types and discrete components were employed which served only a single function.

An established technique for predicting overall reliability of a system involves a computerised FMECA (failure mode and criticality analysis). The problem with such a technique is the necessity to estimate the effect of each possible hardware failure on the executing software in order to predict the probability of a complete system failure or the effect of a partial failure. However, a VLSI circuit cannot realistically be treated as a single component for the purposes of this analysis and the inclusion of each element comprising an integrated circuit is a formidable challenge.

Whilst failure rate models have been developed for a wide range of microcircuits, such models include an unacceptably large number of empirical factors (complexity factors) which attempt to quantify the number of gates, packaging, pin count and type of technology, as well as environmental and temperature effects. The values of these empirical factors are based on analysis of failures in service. As the complexity of circuits grows, it is clear that they can be used in an almost infinitely large number of ways and that not only will the number of possible failure modes become very large but they will depend on the way the circuit is exercised by the software. For example, certain parts of a memory chip could fail totally and the fault not be detected, if those addresses are not normally accessed. Furthermore, the packing density of modern VLSI circuits is becoming so high that considerations such as design rule violation, current densities, heat flows, diffusion, electromigration, etc., become highly important. The precise details of the semiconductor processing now become an important part of the reliability assessment, and it can no longer be assumed that a circuit design which successfully passes through a design rule checker will not fail prematurely.

The possible approaches to failure prediction on VLSI systems include:

(a) the accumulation of failure mode statistics and the use of this information as the basis of the set of empirical parameters;
(b) the analysis of the internal circuit arrangements of the chip and prediction of reliability in terms of component count, track lengths and widths, packaging densities, etc.

Neither of these approaches is in itself sound since VLSI devices are themselves systems and failure studies must necessarily include consideration of how the software interacts with and stresses the hardware. Furthermore, the use of fault-tolerant programming techniques and error-correcting codes will significantly improve the perceived failure rate. A simplistic view would suppose that additional redundant hardware and increased software complexity would lead to degraded reliability.

The present work is aimed at providing sound modelling techniques which allow prediction of the effects of failure and also provide a tool enabling these effects to be properly integrated into the design process.

2 EFFECTS OF INTERCONNECT FAILURES IN VLSI LOGIC CIRCUITS

The results presented here demonstrate failures in integrated circuits which in all respects meet the standard process design rules and which nonetheless fail catastrophically due apparently to track defects. An attempt is made to model the effects of such failures and to demonstrate how their effect may influence the behaviour observed at the terminals.

Fig. 1. Necking at track junctions.
Finally, the effect of marginal input conditions and component values is assessed as a means of characterising premature failure.

2.1 Scanning electron microscope studies

A variety of integrated circuits have been examined, both unstressed and with voltages applied under a scanning electron microscope. A number of defects in the conductors are readily observed including track thinning, necking, whiskers and cracks. Such defects are bound to cause premature failure and could be due to fabrication defects or damage in storage (recent studies demonstrate that 64k DRAMs exhibit metal diffusion whilst in storage). Figure 1 shows necking at a track junction; the decrease in cross-sectional area leads to an increase in current density under normal operating conditions causing premature failure.

In other regions of the integrated circuit there were clear whiskers in the space between the tracks (Fig. 2). When the device is under bias, electromigration effects will further enhance the growth of these defects, leading to centres where open-circuiting of the track, or short circuiting between adjacent tracks and through interlayer dielectrics occurs.

2.2 Modelling and prediction of effects of failure

A powerful and readily available tool for studying the effects of failures is a circuit modelling computer program, such as SPICE, which has...
Fig. 3. TTL inverter circuit (as designed).

Fig. 4. Response of fully functional inverter (transient analysis). Time is in nanoseconds.
Fig. 5. Output waveforms of damaged inverter. (a) T2 failed (transient analysis); (b) open-circuit track (transient analysis). Time is in nanoseconds.
been used in this study. Basic logic circuit elements, for example single gates, and indeed entire integrated circuits can be simulated using this package in a time-domain large-signal mode. To demonstrate the value of this approach a series of studies have been carried out on a simple inverter. In particular, the effects of transistor failure (or low current gain), interconnect failure, and input signals or bias conditions which are out of specification can be studied. Figure 3 illustrates a common circuit arrangement for bipolar TTL inverter commonly used in integrated circuits. The input is a 3.6 V, 18 ns pulse and the circuit is operated off a 5 V supply.

Figure 4 shows the output voltage for a fully functional circuit. The corresponding response for an inverter with one totally failed transistor (T2, zero current gain) shows a marked degradation in performance when an open circuit track is simulated (track metallisation failure at the emitter of T2); the result is such (see Fig. 5) that the circuit no longer functions to the specification, and would in fact produce an erroneous output.

Finally, Fig. 6 demonstrates the effects of marginal supply voltage and indicates the detrimental effect this may have on subsequent stages in a large integrated circuit.

Fig. 6. Effect of marginal bias supply voltage (transient analysis). Time is in nanoseconds.
It is clear that this technique is readily extended to large-scale circuits and can be used for evaluating the overall sensitivity of the circuit performance to the variation in the parameters of the circuit.

3 CONCLUSIONS

A new technique for investigating the effects of failure in VLSI circuits has been described. Preliminary results indicate the usefulness of this approach for providing quantitative information. The advantage of this circuit modelling technique (as opposed to the more traditional phenomenological approach) is that it should enable prediction of possible failure sites, the effects of failure and the consequences of design changes. The use of modified FMECA methods can be used in conjunction with such models to predict the interaction with software, where the criticality of failure at particular points is to be assessed.

REFERENCES